(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 293 156 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88304655.9

(51) Int. Cl.4: H03K 5/15

(22) Date of filing: 23.05.88

(30) Priority: 25.05.87 JP 125925/87
25.05.87 JP 125926/87

(43) Date of publication of application:
30.11.88 Bulletin 88/48

(84) Designated Contracting States:
DE FR GB IT NL

(71) Applicant: CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko
Ohta-ku Tokyo(JP)

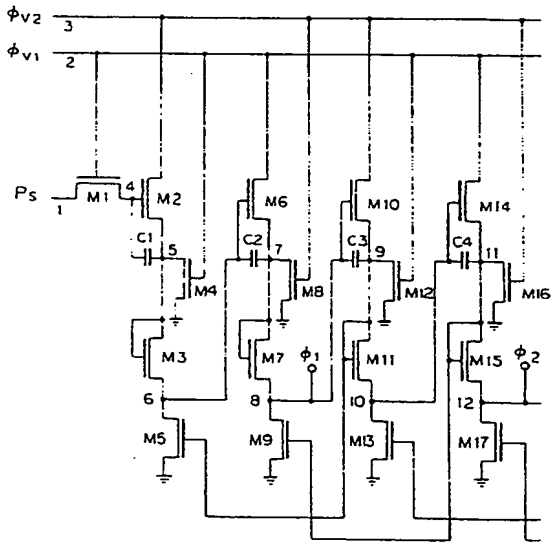
(72) Inventor: Hashimoto, Seiji
6-2-307, Namiki 2-chome Kanazawa-ku
Yokohama-shi Kanagawa-ken(JP)
Inventor: Harada, Tadanori
870-5-1209, Kitahara-cho
Tokorozawa-shi Saitama-ken(JP)

(74) Representative: Beresford, Keith Denis Lewis et al
BERESFORD & Co. 2-5 Warwick Court High Holborn
London WC1R 5DJ(GB)

(54) Scan circuit.

(57) There is provided a scan circuit in which a plurality of unit circuits are connected and scan pulses (ϕ1, ϕ2 ...) are sequentially output from the unit circuits in response to drive pulses (ϕ_{v1}, ϕ_{v2}). In this circuit, the potential (V8, V12...) at an output terminal of the unit circuit is raised by one drive pulse (ϕ_{v1}). The potential at the output terminal is further increased by use of the bootstrap effect (C3...) by the other drive pulse (ϕ_{v2}), thereby forming a scan pulse.

Fig. 2A



EP 0 293 156 A2

BNSDOCID: <EP_____0293156A2_I_>

SCAN CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a scan circuit in which a plurality of unit circuits are connected and scan pulses are sequentially output from the unit circuits in response to drive pulses.

Related Background Art

Fig. 1 is a schematic circuit diagram of a drive section in a solid state image pickup apparatus using a conventional scan circuit.

In the diagram, respective output terminals of a scan circuit 401 are connected to horizontal lines HDL_1, HDL_2, and HDL_3, and to horizontal lines HDL_3, HDL_4, HDL_5, ... through transistors Qy_1 to Qy_4.

A signal F_1 to select odd number fields is input to gate electrodes of the transistors Qy_1 and Qy_2. A signal F_2 to select even number fields is input to gate electrodes of the transistors Qy_3 and Qy_4. Namely, the transistors Qy_1 to Qy_4 constitute an interlacing circuit.

When the signal F_1 is input, scan pulses Qy_1, Qy_2, ... are sequentially output to the horizontal lines HDL_1 and HDL_2, horizontal lines HDL_3, and HDL_4, ... through the transistors Qy_1 and Qy_2.

On the other hand, when the signal F_2 is input, the scan pulses Oy_1, Oy_2, ... are sequentially output to the horizontal lines HDL_2 and HDL_3, the HDL_4 and HDL_5, ... through the transistors Qy_3 and Qy_4.

However, in the foregoing image pickup apparatus using the conventional scan circuit, the signals F_1 and F_2 are transferred to the horizontal lines HDL through the transistors Qy_1 and Qy_2 and the transistors Qy_3 and Qy_4 of the interlacing circuit. Therefore, there are problems such that a voltage drop due to a threshold value voltage Vth of the transistor Qy occurs and the dynamic range is narrowed, so that the picture quality deteriorates.

To solve this problem, in Japanese Patent Gazette No. 61-61586, a vertical buffer circuit to compensate a voltage level of the scan pulse Oy is provided. However, since the buffer circuit is separately provided, the number of elements constituting the vertical scan circuit increases and also the buffer circuit has a bootstrap capacitance. Thus, there is a problem such that it is difficult to reduce the area of the elements.

On the other hand, since two horizontal lines are simultaneously driven, the conventional drive circuit cannot be used in the image pickup devices in which a signal is readout by every one vertical line. Namely, the conventional constitution has problems such that there is a limitation in driving manner and this constitution can be applied to only the limited driving method.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a scan circuit which can output scan pulses of an enough high level without providing any special circuit to compensate a voltage level of the scan pulses.

According to one embodiment of the present invention, there is provided a scan circuit in which a plurality of unit circuits are connected and scan pulses are sequentially output from the unit circuits in response to drive pulses, wherein a potential at an output terminal of the unit circuit is raised by one drive pulse and the potential at the output terminal is further increased by use of the bootstrap effect by another drive pulse, thereby forming the scan pulses.

In this manner, since the scan pulse at a high voltage can be output by use of the bootstrap effect, the voltage drop by the interlacing circuit or the like can be sufficiently compensated. Any special compensating circuit like the conventional circuit is unnecessary. The constitution of the circuit can be simplified and the area of the devices can be easily reduced.

On the other hand, according to another embodiment of the invention, there is provided a drive circuit of a solid state image pickup apparatus for supplying a drive signal to a plurality of drive lines to drive image pickup elements, wherein a switching means are provided for each output of the scan circuit and the a drive signals can be supplied to desired a of the drive lines through the switching means, and the drive signals can be supplied to the drive lines in a desired mode by a desired combination of the scan output of the scan circuit and the a drive signals.

With this constitution, even when a plurality of drive lines are scanned, each line can be independently driven and various kinds of driving modes such as interlacing scan, non-interlacing scan, and the like of a plurality of lines can be easily realized.

The above and other objects and features of

BNSDOCID: <EP_____0293156A2_I_>

the present invention will become apparent from the following detailed description and the appended claims with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram of a drive section in a solid state image pickup apparatus using a conventional scan circuit;

Fig. 2A is a partial circuit diagram in the first embodiment of a scan circuit according to the present invention;

Fig. 2B is a voltage waveform diagram in the respective sections for explaining the operation of the embodiment;

Fig. 3 is a partial circuit diagram of the second embodiment of the invention;

Fig. 4 is a voltage waveform diagram for explaining the operation of the circuit in Fig. 3;

Fig. 5 is a schematic circuit diagram of a drive section using a scan circuit of the embodiment;

Fig. 6 is a timing chart for explaining the operation of the drive section of Fig. 5;

Fig. 7 is a schematic circuit diagram of another example of a drive section using the scan circuit of the embodiment;

Fig. 8 is a timing chart for explaining the operation of the drive section of Fig. 7;

Fig. 9 is a schematic cross sectional view showing an example of a photoelectric converting cell which is used in a solid state image pickup apparatus;

Fig. 10A is an equivalent circuit diagram of the photoelectric converting cell;

Fig. 10B is a voltage waveform diagram for explaining the operation of the circuit of Fig. 10A;

Fig. 11 is a schematic circuit diagram of the image pickup apparatus using the photoelectric converting cell; and

Fig. 12 is a timing chart for schematically explaining the operation of the image pickup apparatus of Fig. 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be described in detail hereinbelow with reference to the drawings.

Fig. 2A is a partial circuit diagram of the first embodiment of a scan circuit according to the invention. Fig. 2B is a voltage waveform diagram in the respective sections for explaining the operation of the embodiment.

In this embodiment, n unit circuits are connected and scan pulses ϕ_1 to ϕ_n are sequentially output from the unit circuits. It is assumed that a potential of each section in Fig. 2A is expressed like V(i) using the number (i) added to each section.

In the diagrams, in the unit circuit at the first stage, when a pulse ϕ_{v1} rises after a pulse P_s was applied, a transistor M_1 is made conductive and the potential V(4) rises. Since the potential V(4) is the gate potential of a transistor M_2, the transistor M_2 shows a conductance corresponding to the potential V(4).

Subsequently, when the pulse ϕ_{v1} falls and a pulse ϕ_{v2} rises, the potential V(5) increases through the transistor M_2. The increase in the potential V(5) is fed back to a gate of the transistor M_2 via a capacitor C_1, thereby increasing the potential V(4) due to the bootstrap effect. The increase in the potential V(4) acts so as to raise a conductance of the transistor M_2. Therefore, the pulse ϕ_{v2} passes, while a voltage drop hardly occurs due to the transistor M_2. This pulse is transmitted through a transistor M_3, thereby increasing the potential V(6).

Since the potential V(6) is the gate potential of a transistor M_6, a conductance of the transistor M_6 rises in correspondence to the potential V(6).

When the pulse ϕ_{v1} subsequently rises, the potential V(7) increases through the transistor M_6. The potential V(6) further rises due to the bootstrap effect owing to the increase in the potential V(7). Since the increase in the potential V(6) acts so as to enhance the conductance of the transistor M_6, the pulse ϕ_{v1} allows the potential V(8) to be raised through the transistors M_6 and M_7 (refer to Fig. 2B). Therefore, a transistor M_{10} exhibits the conductance corresponding to the gate potential V(8).

Next, when the pulse ϕ_{v2} rises, the transistor M_8 is turned on and the potential V(7) is reset to the earth potential and the transistor M_7 is turned off. Thus, the portion of the potential V(8) is set into the floating state.

At the same time, since the pulse ϕ_{v2} rises, the potential V(9) rises through the transistor M_{10}. The increses in the potential V(9) further increases the potential V(8) by the bootstrap effect.

If such a change in the potential V(8) is used as a scan pulse ϕ_1, a scan pulse at a high voltage can be obtained.

Next, the potential V(8) is reset by the pulse ϕ_{v1} and at the same time, the potential V(12) rises and, further, increases by the subsequent pulse ϕ_{v2}. The potential V(12) is used as a scan pulse ϕ_2. In a manner similar to the above, scan pulses ϕ_3 to ϕ_n at a high voltage level are successively output synchronously with the pulses ϕ_{v2}.

In Fig. 2B, by properly setting the timings for the drive pulses ϕ_{v1} and ϕ_{v2}, the waveforms of the

BNSDOCID: <EP_____0293156A2_I_>

scan pulses ϕ_1 to ϕ_n can be made approach a square shape.

Fig. 3 is a partial circuit diagram of the second embodiment of the invention. Fig. 4 is a voltage waveform diagram for explaining the operation thereof.

In this embodiment, first, the transistor M_1 is turned on and the potential V(A) rises by the start pulse P_s and drive pulse ϕ_{v1}. Thus, the transistors M_2 and M_3 exhibit a certain conductance.

Subsequently, since the drive pulse ϕ_{v1} falls, an output of an inverter 501 rises. Consequently, a voltage is applied to a capacitor C_p through the transistor M_3 and the potential V(A) further rises by the bootstrap effect.

Therefore, if such a change in the potential V-(A) is used as a scan pulse ϕ_1, the scan pulse at a high voltage can be derived in a manner similar to the first embodiment. In a manner similar to the above, scan pulses ϕ_2 to ϕ_n at a high voltage level can be successively output synchronously with the drive pulses ϕ_{v1} and ϕ_{v2}.

Therefore, even when the interlacing circuit shown in Fig. 1 is provided, the voltage drop can be sufficiently compensated and the high level drive voltage can be transferred to the horizontal lines HDL.

Fig. 5 is a schematic circuit diagram of a drive section using the scan circuit of the embodiment. Fig. 6 is a timing chart for explaining the operation thereof.

As shown in Fig. 5, the image pickup device comprises photoelectric converting cells C_{11}, C_{12}, ... and the like which are arranged like an area and driven every row by the horizontal lines HDL_1, HDL_2, HDL_3, ... The photoelectric conversion signals are read out through the vertical lines and transistors Q_1 and Q_2.

In this embodiment, gate electrodes of three transistors Q_{v1} to Q_{v3} are connected to output terminals of a scan circuit 101, respectively.

Each transistor Q_{v1} transfers a drive voltage V_{r1} to the horizontal lines HDL_1, HDL_3, HDL_5, ... Each transistor Q_{v2} transfers a drive voltage V_{r2} to the horizontal lines HDL_2, HDL_4, HDL_6, ... Each transistor Q_{v3} transfers a drive voltage V_{r3} to the HDL_3, HDL_5, HDL_7, ...

In such a circuit arrangement, the scan circuit 101 sequentially outputs the scan pulses ϕ_1, ϕ_2, ... in response to pulses ϕ_{v1} and ϕ_{v2} Therefore, by applying the drive voltages V_{r1} to V_{r3} by a proper combination, the image pickup device can be scanned in a desired mode.

For example, as shown in Fig. 6, by applying the drive voltage V_{r1} and V_{r2} in the odd number fields, the horizontal lines HDL_1 and HDL_2, and HDL_3 and HDL_4, ... are driven and by applying the drive voltage V_{r2} and V_{r3} in the even number fields, the HDL_2 and HDL_3, and HDL_4 and HDL_5, ... are driven. In this manner, the interlacing scan of the two line driving type can be accomplished.

On the other hand, if the drive voltages V_{r1} and V_{r2} and the drive voltages V_{r2} and V_{r3} are applied at different timings which are deviated from each other, the vertical line of the image pickup device can be also set to a single vertical line.

Even when such a vertical buffer circuit is provided, since the output of the scan circuit 101 according to the embodiment is set to the high voltage level, the transistors Q_{v1} to Q_{v3} can be set to enough high conductances. The drive voltages V_{r1} to V_{r3} can be transferred to the horizontal lines HDL without reducing the drive voltages V_{r1} to V_{r3}.

Fig. 7 is a schematic circuit diagram of another example of a drive section using the scan circuit of the embodiment. Fig. 8 is a timing chart for explaining the operation thereof.

In this manner, by providing the transistors Q_{v1} to Q_{v4} at the respective output terminals of the scan circuit 101 and by combining the drive voltages V_{r1} to V_{r4} as shown in the timing chart, the interlacing scan of the three-line driving type can be also accomplished.

A practical example of a solid state image pickup apparatus using the embodiment will now be explained.

Fig. 9 is a schematic cross sectional view of an example of photoelectric converting cells which are used in the solid state image pickup apparatus.

In the diagram, an n^- layer 202 serving as a collector region is formed on an n type silicon substrate 201 by the epitaxial growth. A p base region 203 is formed in the n^- layer 202. An n^+ emitter region 204 is further formed in the p base region 203. In this manner, a bipolar transistor is constituted.

The p base region 203 is two-dimensionally arranged. The cells in the horizontal direction are separated from the cells in the vertical direction by a device separating region. Although not shown, the device separating region comprises an oxide film formed by the LOCOS oxidation and an n^+ region formed under the oxide film.

On the other hand, a gate electrode 208 is formed between horizontally neighboring p base regions 203 through an oxide film 207. Therefore, a p channel MOS transistor in which the adjacent p base regions 203 are used as source and drain regions is constituted.

This MOS transistor is the normally OFF type and is set to the OFF state when the potential of the gate electrode 208 is the earth potential or positive potential. Therefore, the p base regions 203 between the adjacent cells are electrically isolated. On the contrary, when the potential of the gate electrode 208 is a negative potential which

EPODOC: <EP_____0293156A2_I_>

exceeds a threshold value potential V_{th}, the MOS transistor is set to the ON state, so that the p base regions 203 of the respective cells are mutually made conductive.

The gate electrodes 208 are commonly connected to the drive line every row in the horizontal direction. Further, capacitors 209 to control the potentials of the p base regions 203 are also similarly connected to the drive line. The drive line extends in the horizontal direction on the oxide film serving as the device separating region.

Further, after a transparent insulative layer 211 was formed, an emitter electrode 212 is formed. The emitter electrodes 212 are connected to a vertical line 213 every column. A collector electrode 214 is formed on the back surface of the substrate 201 through an ohmic contact layer.

Fig. 10A is an equivalent circuit diagram of the photoelectric converting cell. Fig. 10B is a voltage waveform diagram for explaining the operation thereof.

It is now assumed that carriers (in this case, holes) as much as the incident light amount are accumulated in the p base region 203. It is also assumed that a negative voltage V_c is applied to a terminal of a transistor Q_c and a positive voltage is applied to the collector electrode 214.

In this state, pulses ϕ_d of a positive voltage are applied to a drive line 210 for only a period of time T_{rd}. Thus, the potential of the p base region 203 rises through a capacitor C_{ox} and the signal is read out to the emitter electrode 212 as mentioned above.

Subsequently, pulses ϕ_d of a negative voltage are applied to the drive line 210 for only a period of time T_{rh}. Thus, the p channel MOS transistor Q_c is turned on and the base potential is reset to the voltage V_c and the refreshing operation is completely performed. On the other hand, by setting a pulse ϕ_r to the high level, the transistor Q_r is turned on, thereby resetting the vertical line 213.

As already mentioned above, as the refreshing operation, after the MOS transistor Q_c was turned on, the pulse ϕ_d of a positive voltage can be also applied while the emitter electrode 212 is grounded. In this case, there is no need to set the voltage V_c to a negative voltage but can be set to the earth voltage or positive voltage.

After completion of the foregoing refreshing operation, the accumulating operation is started. The similar operations are repeated hereinafter.

Fig. 11 is a schematic circuit diagram of an image pickup apparatus using the foregoing photoelectric converting cells.

In this apparatus, m x n photoelectric converting cells are arranged like an area.

In the cells C_{11} to C_{1n}, C_{21} to C_{2n}, ... on the horizontal lines, the gate electrodes 208 of the MOS transistor Q_c are commonly connected to the drive lines HDL_1 to HDL_m, respectively.

The drive lines HDL_1 to HDL_m are connected to a vertical buffer circuit 301. The scan pulses ϕ_1 to ϕ_m are input to the vertical buffer circuit 301 from the vertical scan circuit 101 as the embodiment.

The MOS transistors Q_c in each of which the p base regions 203 in each cell are used as source and drain regions are serially connected every horizontal line. The p regions to form the MOS transistor Q_c are respectively formed in the cells C_{11} to C_{m1} arranged at the edge line. On the other hand, MOS transistors Q_{x1} to Q_{xm} are respectively serially connected to the cells C_{1n} to C_{mn}. A constant voltage V_c is applied to both ends.

The emitter electrodes in the cells C_{11} to C_{m1}, C_{12} to C_{m2}, ... in the vertical direction are commonly connected to vertical lines VL_1 to VL_n, respectively. The vertical lines are grounded through reset transistors Q_{r1} to Q_{rn}. A reset pulse ϕ_r is commonly input to the gate electrodes of the transistors Q_{r1} to Q_{rn}.

The vertical lines VL_1 to VL_n are connected to capacitors C_1 and C_2 through transistors Q_{t1} and Q_{t2}, respectively. The pulses ϕ_1 and ϕ_2 are input to the gate electrodes of the transistors Q_{t1} and Q_{t2}.

Further, the capacitors C_1 and C_2 are connected to signal lines 303 and 304 through the transistors Q_1 and Q_2, respectively. Scan pulses ϕ_{11} to ϕ_{n1} of a horizontal scan circuit 302 are input to the gate electrodes of the transistors Q_1 and Q_2, respectively.

Various kinds of pulses ϕ, voltages V, and the like to drive the image pickup apparatus are supplied from a driver 305. The driver 305 is controlled by a controller 306.

Fig. 12 is a timing chart for schematically explaining the operation of the image pickup apparatus.

In the odd number fields F_o, when the pulses ϕ_{v1} and ϕ_{v2} are input to the vertical scan circuit 101, the scan pulse ϕ_1 rises. The scan pulse ϕ_1 is set to the high voltage since it uses the bootstrap effect as mentioned above.

Thus, the vertical buffer circuit 301 outputs input voltages $V_{r1}$and V_{r2} to the horizontal lines HDL_1 and HDL_2, respectively.

Simultaneously with the rising of the pulse ϕ_{v2}, the pulses ϕ_{t1} and ϕ_r rise and the transfer transistor Q_{t1} and reset transistor Q_r are turned on, thereby clearing the vertical lines VL and capacitor C_1.

Subsequently, after the reset transistor Q_r was turned off, the input voltage V_{r1} is set to a positive voltage and the reading operations of the cells C_{11} to C_{1n} on the horizontal line HDL_1 are executed. The readout signals are stored into the capacitor C_1 through the transfer transistor Q_{t1}, respectively.

BNSDOCID: <EP_____0293156A2_I_>

Next, when the pulses ϕ_{t2} and ϕ_r rise, the transfer transistor Q_{t2} and reset transistor Q_r are turned on, thereby clearing the capacitor C_2 and vertical lines VL.

Subsequently, the input V_{r2} is set to a positive voltage and the reading operations of the cells C_{21} to C_{2n} on the horizontal line HDL_2 are executed. The readout signals are stored into the capacitor C_2 through the transfer transistor Q_{t2}.

The foregoing operations are performed within a horizontal blanking period HBLK. Next, the sensor signals of the first and second rows which were accumulated in the capacitors C_1 and C_2 within the effective horizontal period are scanned and output.

Namely, the transistors Q_1 and Q_2 are sequentially turned on by the scan pulses ϕ_{11} to ϕ_{n1} which are successively output from the horizontal scan circuit 302. The signals stored in the capacitors C_1 and C_2 are read out and output to the signal lines 303 and 304.

In parallel with those operations, the pulse ϕ_r rises and the transistor Q_r is turned on, thereby grounding the vertical lines VL. On the other hand, the input voltages V_{r1} and V_{r2} are set to a negative voltage, thereby refreshing the cells of the first and second rows. That is, the MOS transistor Q_c of each cell are turned on and each base potential is set to a constant value.

Next, the input voltages V_{r1} and V_{r2} are set to a positive voltage, thereby refreshing the base regions 203 which were reset to a constant potential. In other words, since the emitter electrodes of the cells are grounded through the vertical lines VL, when a positive voltage is applied to capacitors C_{ox}, the circuit between the base and emitter is forwardly biased, so that the carriers accumulated in the base region 203 are extinguished in a manner similar to the reading operations.

After completion of the refreshing operation in this manner, the cells of the first and second rows start the accumulating operation.

In a manner similar to the above, the reading and refreshing operations of the third and fourth rows, the fifth and sixth rows, ... in the odd number fields F_o are sequentially executed by the pulses ϕ_{v1} and ϕ_{v2}.

In the even number fields F_e, the reading and refreshing operations of the second and third rows, the fourth and fifth rows, ... are successively performed by the input V_{r2} and V_{r3}.

By using the scan circuit 101 according to the embodiment of the invention in the drive section of the image pickup apparatus, the good picture quality can be derived without providing any special voltage level compensating circuit or the like.

As explained in detail above, according to the scan circuit of the invention, the scan pulse can be set to a high voltage level by use of the bootstrap effect. Thus, even when the interlacing circuit or the like is provided, the scan can be performed by an enough high voltage.

Thus, there is no need to compensate the output level by adding the bootstrap capacitance as in the conventional apparatus. The circuit constitution is simplified and the area of the elements can be easily reduced.

According to the drive circuit of the invention, since the drive signals are supplied to the drive lines in a desired mode on the basis of the scan output of the scan circuit and a desired combination of the drive signals, even when a plurality of drive lines are scanned, they can be independently driven. Various kinds of driving modes such as interlacing scan, non-interlacing scan, and the like of a plurality of lines can be easily performed.

Claims

1. A scan circuit in which a plurality of unit circuits are connected and scan pulses are sequentially output form said unit circuits in response to drive pulses,

wherein a potential at an output terminal of the unit circuit is raised by one of the drive pulse and the potential at said output terminal is further raised by using a bootstrap effect by another drive pulse, thereby forming a scan pulse.

2. A scan circuit according to claim 1, wherein said unit circuit has a plurality of transistors.

3. A scan circuit according to claim 2, wherein said unit circuits respectively have input terminals and each of said unit circuits has a first transistor whose gate is connected to said input terminal.

4. A scan circuit according to claim 3, wherein a capacitor is provided between the gate and source of said first transistor.

5. A scan circuit according to claim 3, wherein said output terminal of the unit circuit at the front stage and said input terminal of the unit circuit at the next stage are connected.

6. A unit circuit for use in a shift register comprising:

a) a first transistor whose gate electrode is connected to an input terminal of the unit circuit;

b) a capacitor arranged between the gate electrode and source electrode of said first transistor;

c) a first signal source connected to a drain electrode of said first transistor;

d) a second transistor whose drain electrode is connected to the source electrode of the first transistor, the source electrode of said second transistor being connected to an earth and a gate electrode of the second transistor being connected to a second signal source;

BNSDOCID: <EP_____0293156A2_I_>

e) a third transistor whose gate electrode and drain electrode are connected to the source electrode of the first transistor, a source electrode of said third transistor being connected to a drain electrode of a fourth transistor, a source electrode of said fourth transistor being connected to an earth, and a gate electrode of said fourth transistor being connected to a third signal source; and

f) a signal output terminal for outputting a signal of the gate electrode of said first transistor to the outside of the shift register.

7. A unit circuit according to claim 6, the signal at said output terminal is connected to the drain electrode of said fourth transistor of the unit circuit at the front stage.

8. A solid state image pickup apparatus comprising:

a) a plurality of photosensitive cells arranged in a row and column shape;

b) a selecting line to select the photosensitive cells on a predetermined row from among said plurality of photosensitive cells;

c) scanning means for supplying an address signal to said selecting line, said scanning means having a plurality of stages and output signals being sequentially output one by one from said stages;

d) switching means each including three or more switching elements which are connected to outputs of each stage of said scanning means and are controlled, and said switching elements being connected to said selecting line, respectively; and

e) another control means different from said scanning means, said cotnrol means being provided to control the operations of said three or more switching elements.

9. An apparatus according to claim 8, wherein the selecting line which is controlled by said three or more switching elements connected to a predetermined stage of said scanning means and the selecting line which is controlled by the three or more switching elements connected to another stage adjacent to said predetermined stage are mutually partially overlapped.

10. A scan circuit having a series of circuit stages which are sequentially activated each in response to a clock signal and activation of a preceding stage in the series, wherein each stage has a transistor which is driven on by a signal from the respective preceding stage and which is driven further on by the clock signal.

11. A scan circuit having a series of circuit stages which are sequentially activated each in response to a clock signal and an output signal from a preceding stage in the series, wherein activation of each stage is operable to increase the output signal of the respective preceding signal.

BNSDOCID: <EP 0293156A2_I_>

Fig. 1

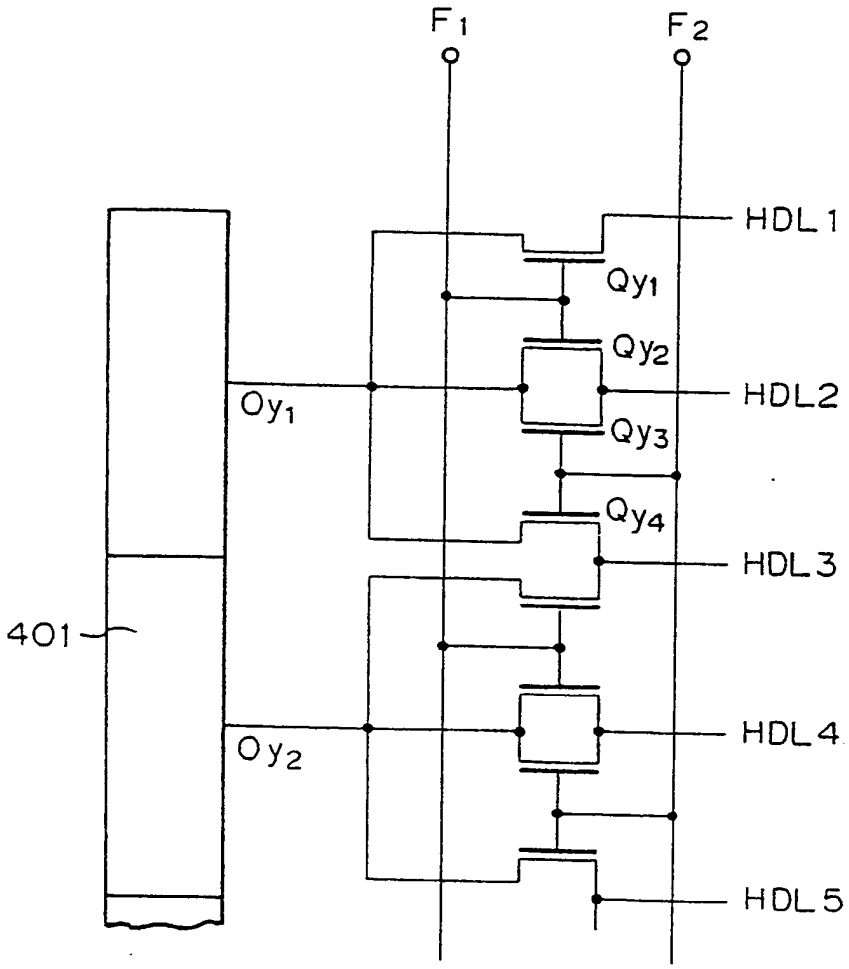
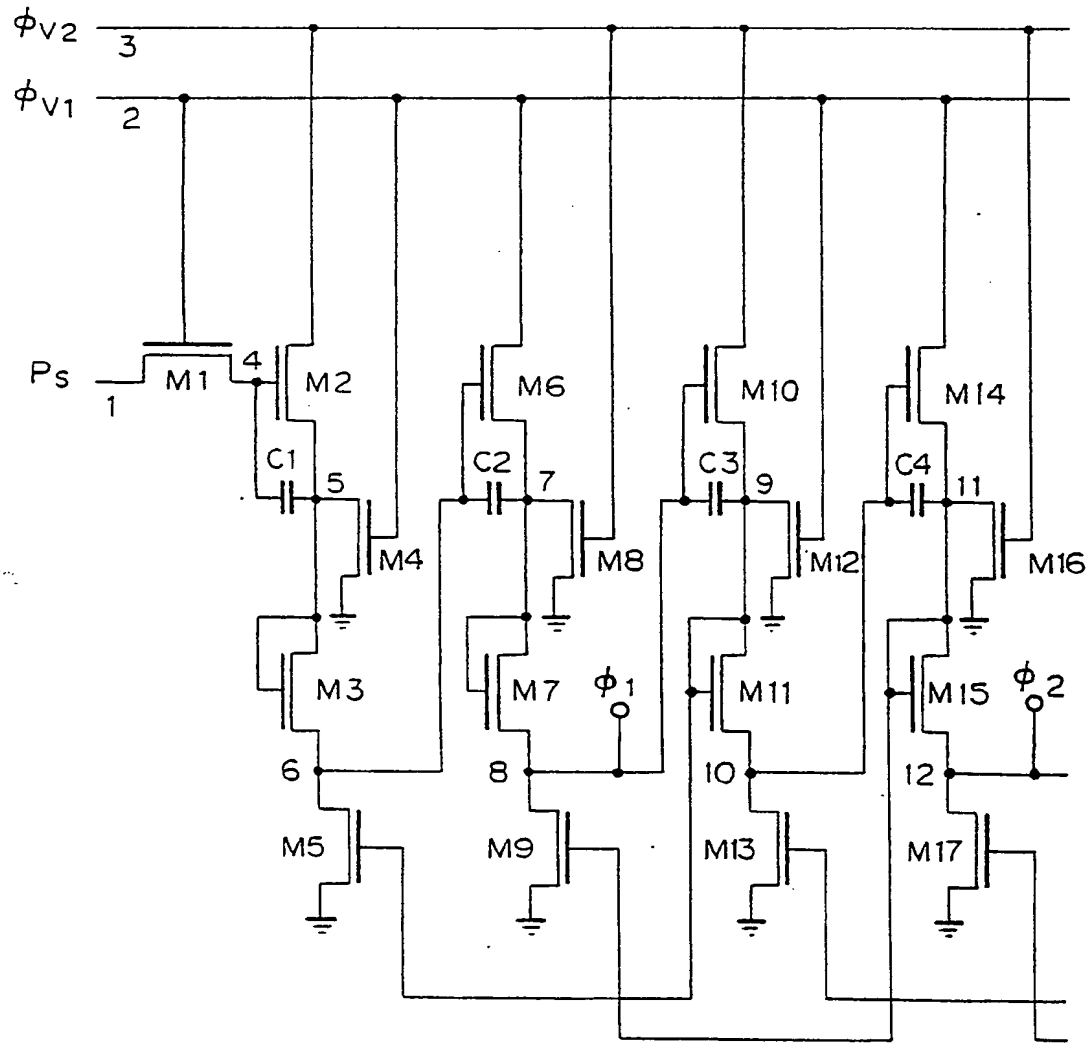
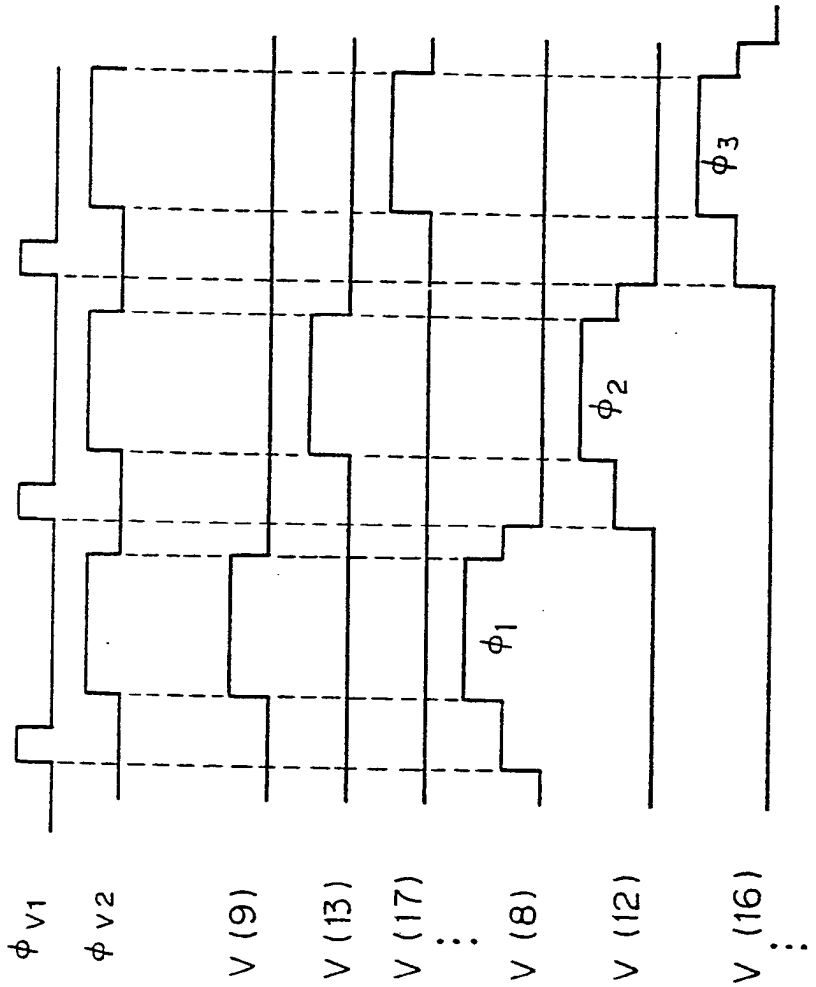


Fig. 2A



BNSDOCID: <EP_____0293156A2_I_>

Fig. 2B



BNSDOCID: <EP_____0293156A2_I_>

Fig. 3

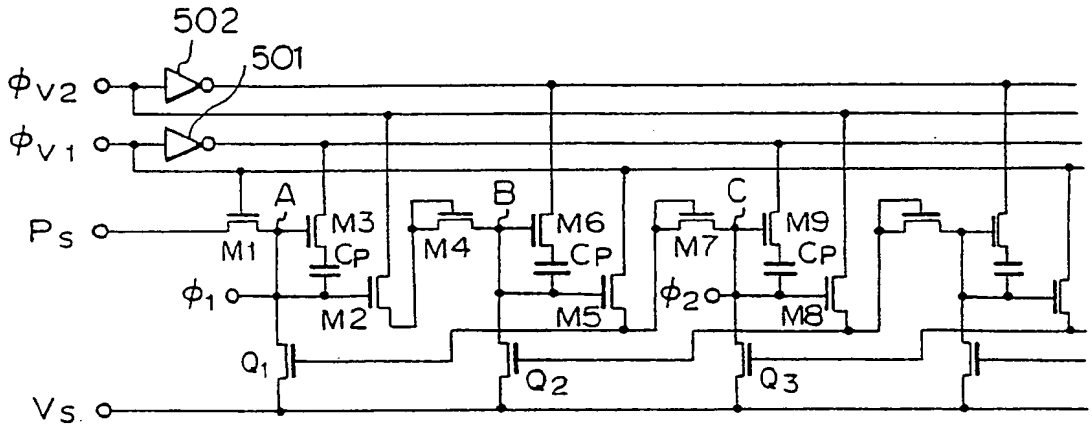
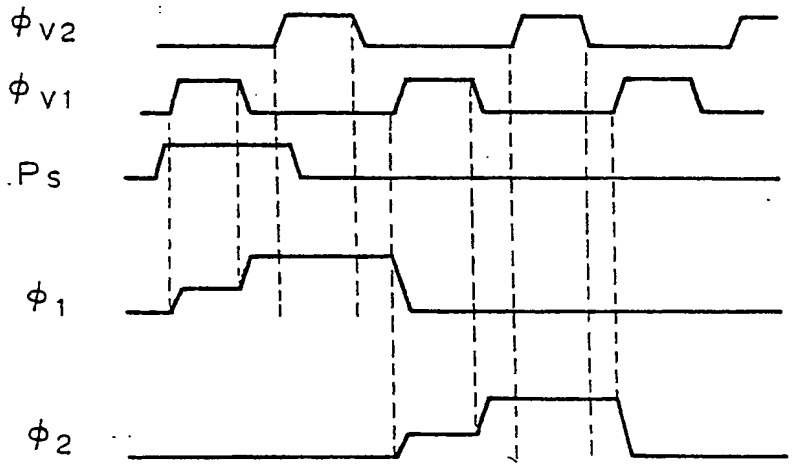


Fig. 4



BNSDOCID: <EP_____0293156A2_I_>

Fig. 5

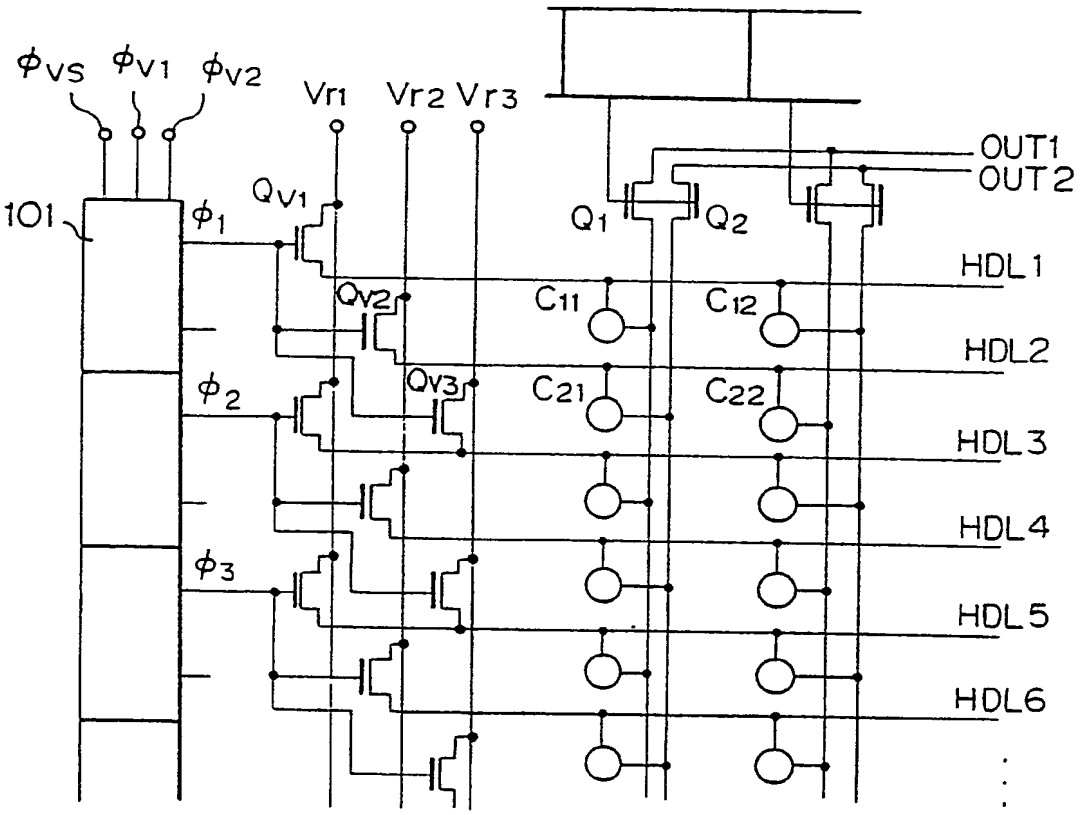
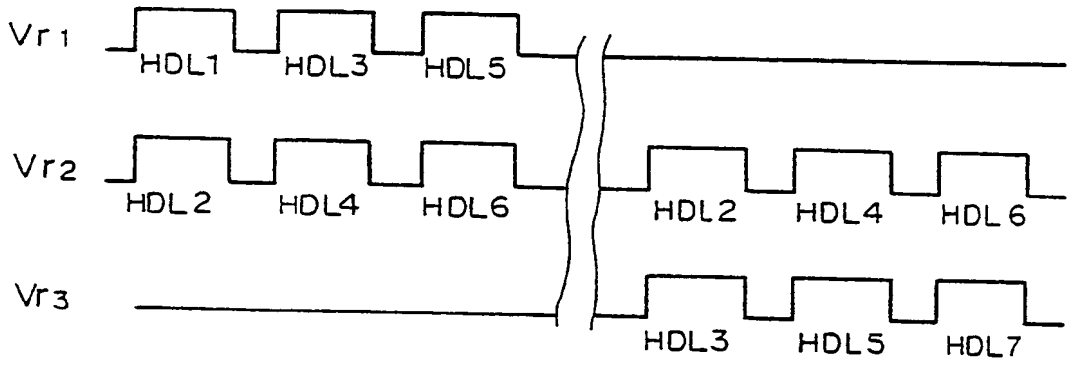


Fig. 6



NSDOCID: <EP_____0293156A2_I_>

Fig. 7

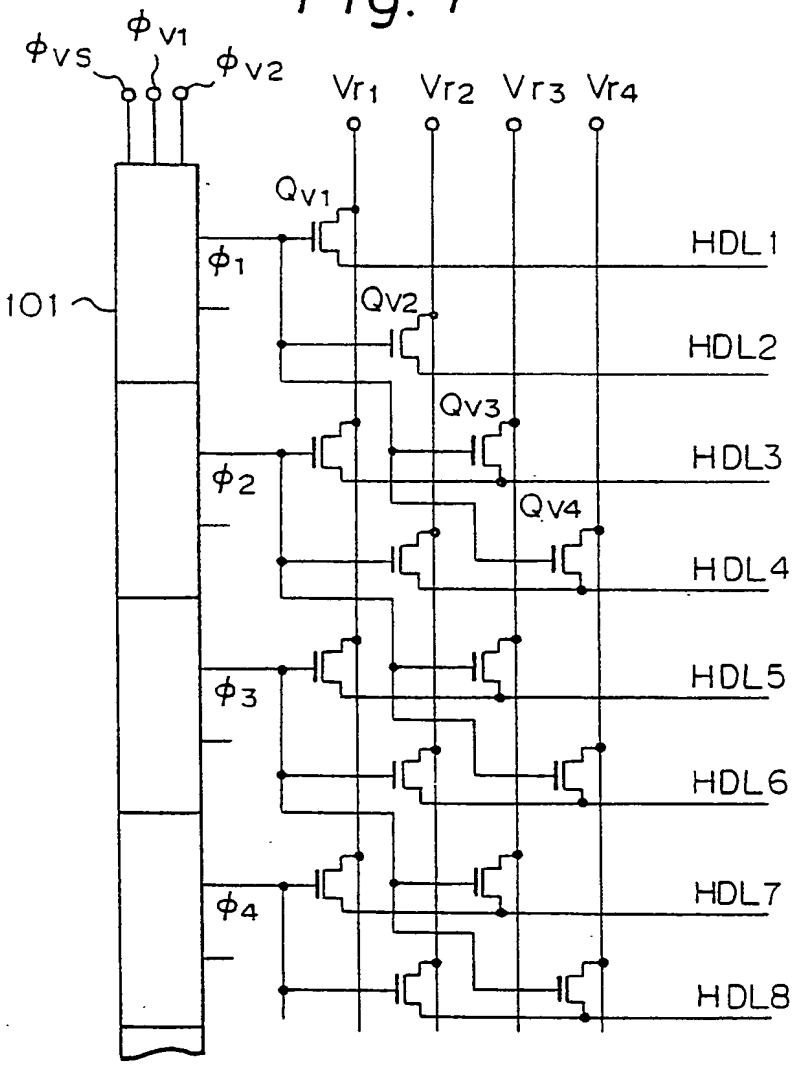
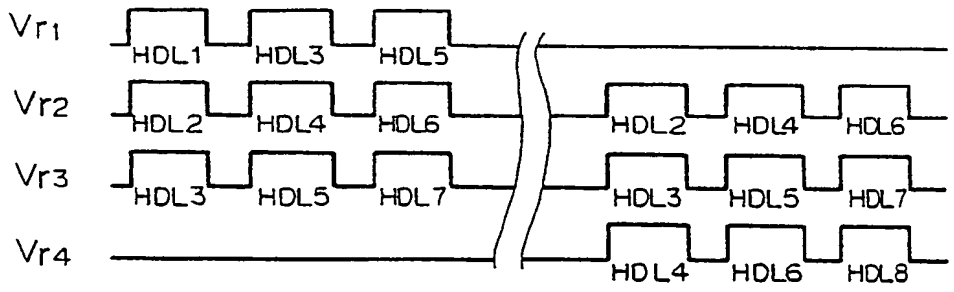


Fig. 8



BNSDOCID: <EP_____0293156A2_I_>

Fig. 9

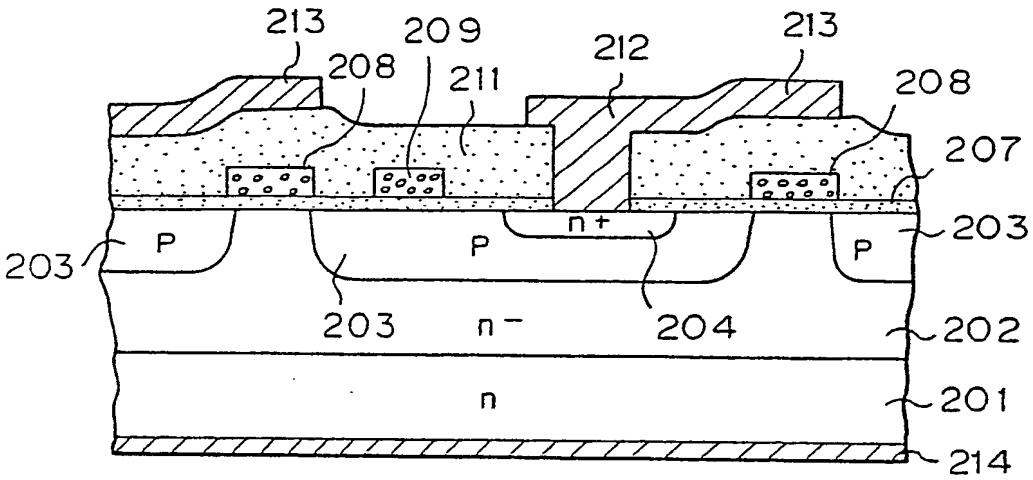


Fig. 10A

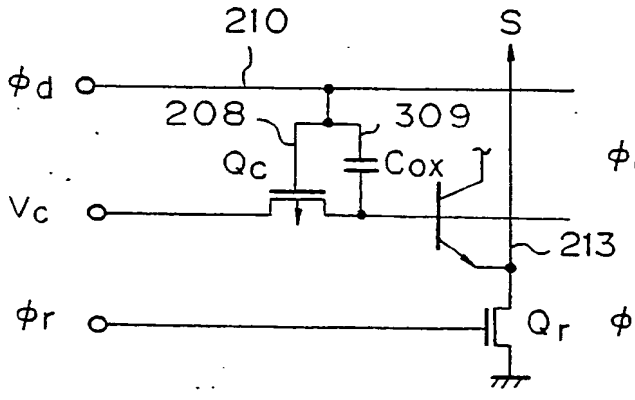
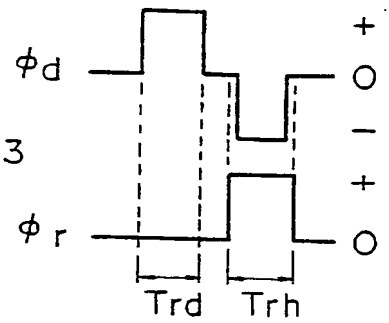


Fig. 10B



ENSDOCID: <EP_____0293156A2_I_>

Fig. 11

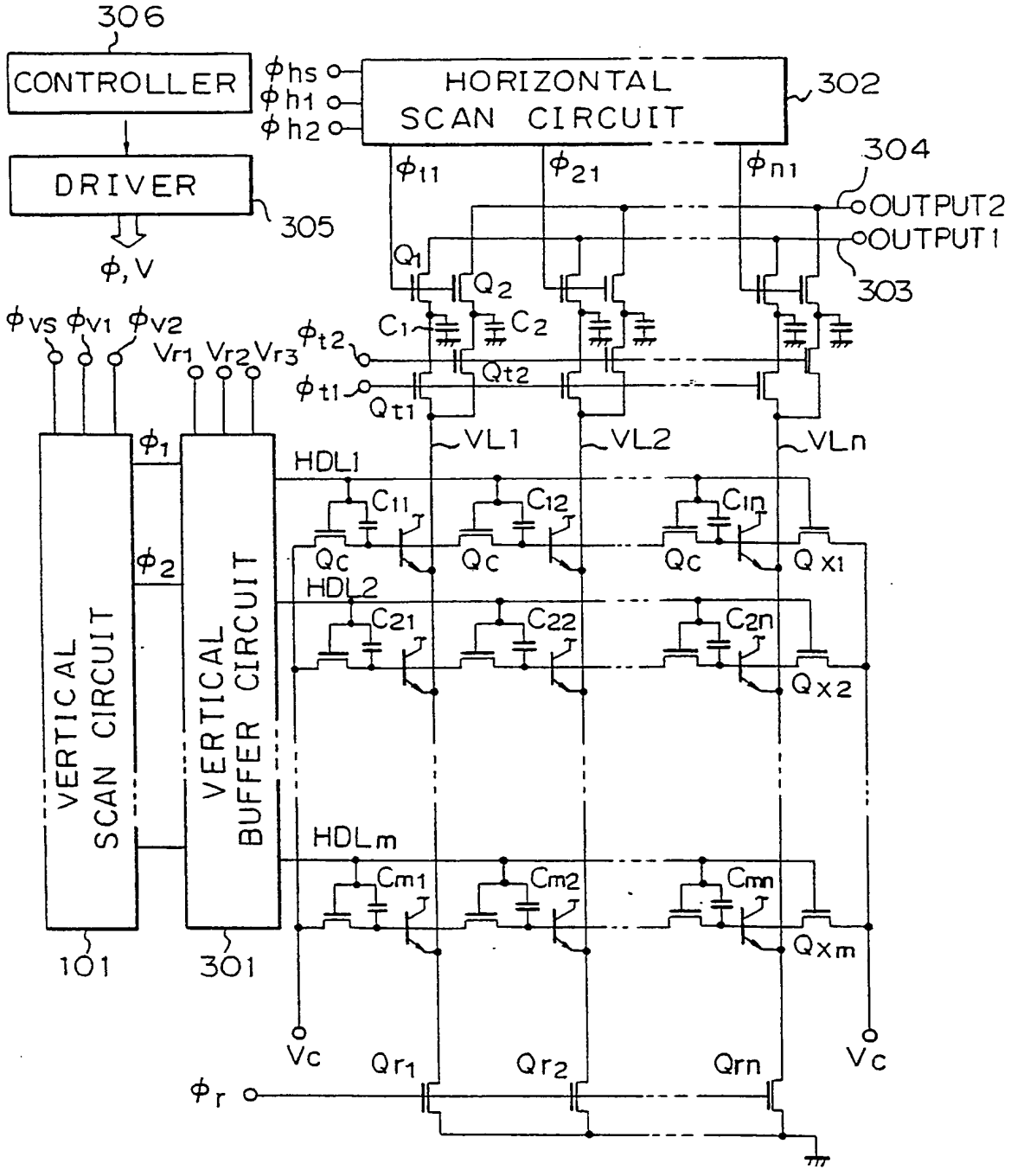
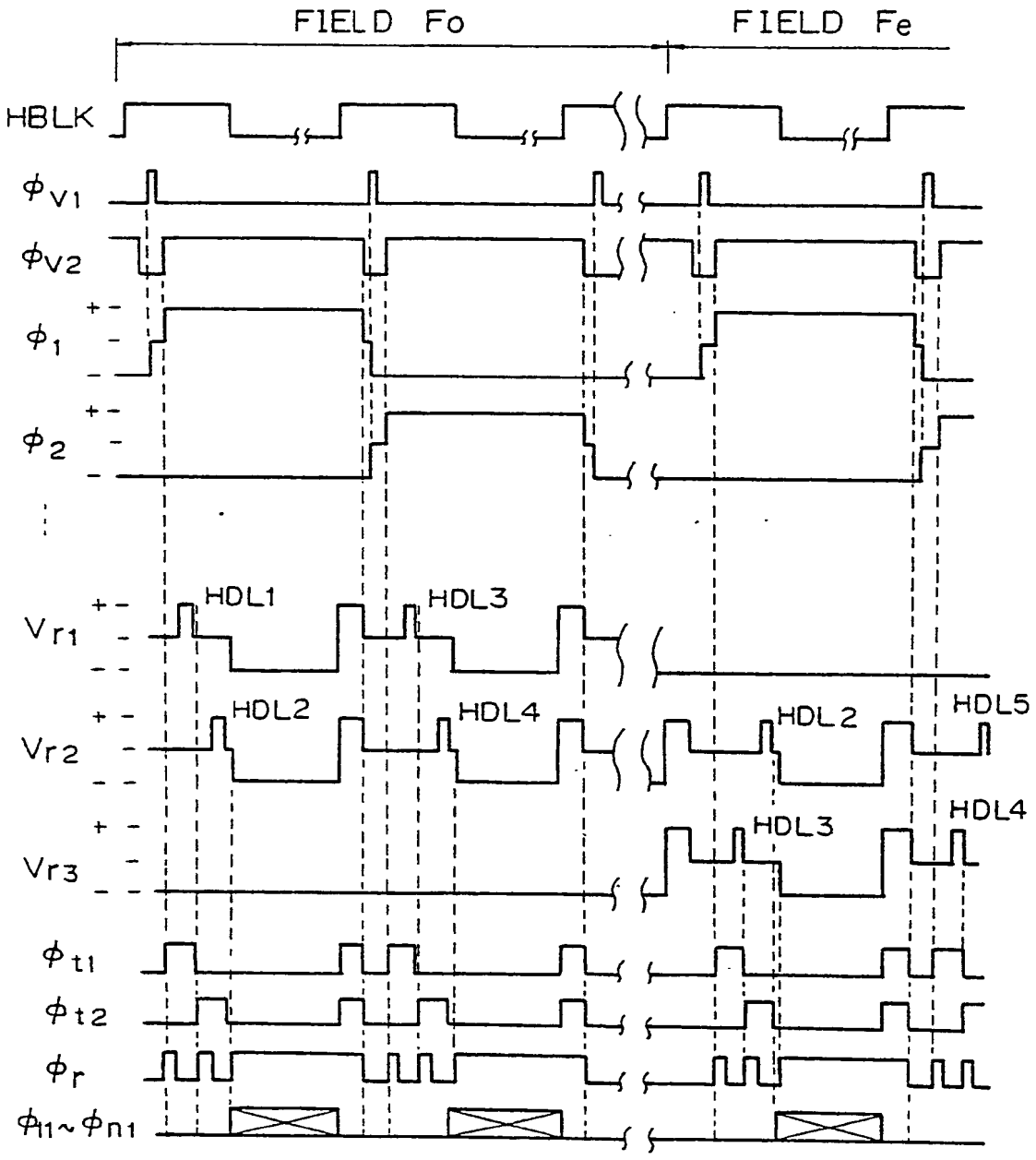

306
CONTROLLER
DRIVER
305
φ, V
φhs
φh1
φh2
HORIZONTAL SCAN CIRCUIT
302
304
OUTPUT2
OUTPUT1
303
φ11
φ21
φn1
Q1
Q2
C1
C2
φvs φv1 φv2
Vr1 Vr2 Vr3
φt2
φt1
Qt2
Qt1
VL1
VL2
VLn
φ1
φ2
HDL1
HDL2
HDLm
C11
C12
C1n
C21
C22
C2n
Cm1
Cm2
Cmn
Qc
Qx1
Qx2
Qxm
VERTICAL SCAN CIRCUIT
VERTICAL BUFFER CIRCUIT
101
301
Vc
Qr1
Qr2
Qrn
φr

Fig. 12



BNSDOCID: <EP_____0293156A2_I_>

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 293 156 A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88304655.9

(22) Date of filing: 23.05.88

(51) Int. Cl.4: H 03 K 5/15

(30) Priority: 25.05.87 JP 125925/87
25.05.87 JP 125926/87

(43) Date of publication of application:
30.11.88 Bulletin 88/48

(84) Designated Contracting States: DE FR GB IT NL

(88) Date of deferred publication of search report:
06.09.89 Bulletin 89/36

(71) Applicant: CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko
Ohta-ku Tokyo (JP)

(72) Inventor: Hashimoto, Seiji
6-2-307, Namiki 2-chome Kanazawa-ku
Yokohama-shi Kanagawa-ken (JP)

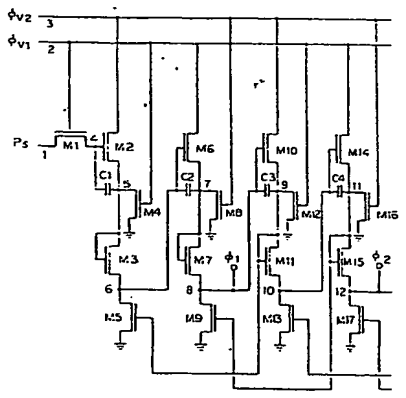
Harada, Tadanori
870-5-1209, Kitahara-cho
Tokorozawa-shi Saitama-ken (JP)

(74) Representative: Beresford, Keith Denis Lewis et al
BERESFORD & Co. 2-5 Warwick Court High Holborn
London WC1R 5DJ (GB)

(54) Scan circuit.

(57) There is provided a scan circuit in which a plurality of unit circuits are connected and scan pulses (φ1, φ2 ...) are sequentially output from the unit circuits in response to drive pulses (φ_{V1}, φ_{V2}). In this circuit, the potential (V8, V12...) at an output terminal of the unit circuit is raised by one drive pulse (φ_{V1}). The potential at the output terminal is further increased by use of the bootstrap effect (C3...) by the other drive pulse (φ_{V2}), thereby forming a scan pulse.

Fig. 2A



EP 0 293 156 A3

BNSDOCID: <EP_____0293156A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 4655

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	GB-A-2 022 953 (HITACHI LTD) * Figure 18; whole document * ---	1-7,10-11	H 03 K 5/15 G 11 C 19/18
X	US-A-3 786 281 (KOIKE et al.) * Figures 6-7; column 1, line 61 - column 2, line 14 * -----	8-9	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 03 K
G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15-06-1989	SEGAERT P.A.O.M.P.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

BNSDOCID: <EP_____0293156A3_I_>